Novel and Efficient 4:2 and 5:2 Compressors with Minimum number of Transistors Designed for Low-Power Operations

Pallavi Devi Gopineedi, Himanshu Thapliyal, M.B Srinivas and Hamid R. Arabnia[1]
Center for VLSI and Embedded System Technologies
International Institute of Information Technology, Hyderabad-500019, India
[1]The University of Georgia, Department of Computer Science,
415 Graduate Studies Research Center, Athens, Georgia 30602-7404, U.S.A

ABSTRACT

This paper proposes efficient and optimal 4:2 and 5:2 compressors. The compressors are highly optimized in terms of transistor count. These designs have the principle advantage that in addition to reduced transition activity, they have no direct connections to the power-supply and is totally driven by the input signals, leading to a noticeable reduction in short-circuit power consumption. The proposed 4-2 and 5-2 compressor designs have been implemented with a bare minimum of 20 and 30 transistors respectively.

Keywords: 4-2 Compressor, 5-2 Compressor and Multipliers.

1. INTRODUCTION

Multiplication is the basic arithmetic operation important in several microprocessors and digital signal processing applications. Digital Signal processing Systems require multipliers to implement DSP algorithms such as convolution and filtering where the multiplier lies directly within the critical path. Hence, the demand for high speed multipliers has become prominent. The enhanced speed leads to increased power consumption, thus, power saving architectures turn to be the choice of the future. This has given way to the development of novel circuit techniques, with the aim of reducing the power dissipation of multipliers without compromising the speed and performance.

A multiplier can be divided into three stages: Partial products generation stage, partial products addition stage, and the final addition stage. In the first stage, the multiplicand and the multiplier are multiplied bit by bit to generate the partial products. The second stage is the most important, as it is the most complicated and determines the speed of the overall multiplier. The 4-2 and 5-2 compressors have been widely employed in the high speed multipliers to lower the latency of the partial product accumulation stage. Owing to its regular interconnection, the 4-2 compressor is ideal for the construction of regularly structured Wallace tree [1,2,3] with low complexity.

In high-speed designs, the Wallace tree construction method is usually used to add the partial products in a tree-like fashion in order to produce two rows of partial products that can be added in the last stage. The Wallace tree is fast since the critical path delay is proportional to the logarithm of the number of bits in the multiplier. There exist a handful of ways to construct the Wallace Tree. The prominent method considers all the bits in each column at a time and compresses them into two bits (a sum and a carry). The Wallace tree is constructed by considering all the bits in each fours row at a time and compressing them in an appropriate manner. Thus, compressors form the essential requirement of high speed multipliers. The speed, area and power consumption of the multipliers will be in direct proportion to the efficiency of the compressors. Thus, in order to satisfy the requirement of small area low power high throughput circuitries, this paper provides novel designs of 4:2 and 5:2 compressors with minimum number of transistors. The proposed designs are highly efficient in terms of small area low power and high throughput. The details of the proposed designs are mentioned in detail in the upcoming sections.

2. 4-2 COMPRESSOR

The 4:2 compressor structure actually compresses five partial products bits into three [1,2,3]. The architecture is connected in such a way that four of the inputs are coming from the same bit position of the weight j while one bit is fed from the neighboring position j-1(known as carry-in). The outputs of 4:2 compressor consists of one bit in the position j and two bits in the position j+1.This structure is called compressor since it compresses four partial products into

two(while using one bit laterally connected between adjacent 4:2 compressors). Figure 1 shows the block diagram of 4-2 compressor. A 4-2 compressor can also be built using 3-2 compressors. It consists of two 3-2 compressors (full adders) in series and involves a critical path of 4 XOR delays as shown in Figure 2. An alternative implementation is shown in Figure 3. This implementation is better and involves a critical path delay of three XOR's , hence reducing the critical path delay by 1 XOR. The output Cout, being independent of the input Cin accelerates the carry save summation of the partial products .

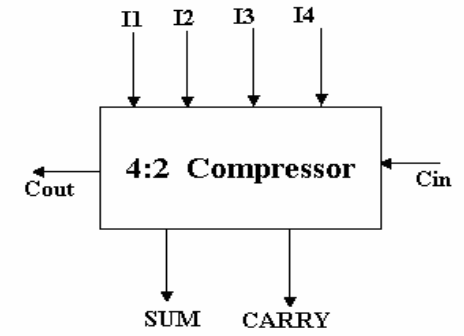

Figure 1. Block Diagram of 4:2 Compressor

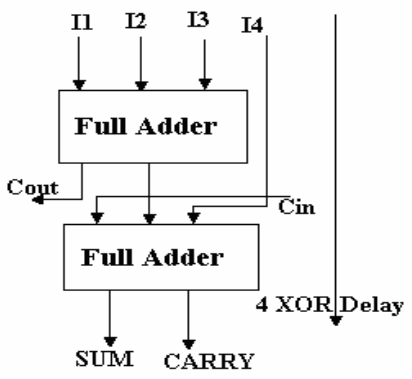

Figure 2. 4:2 Compressor Design using Full Adders

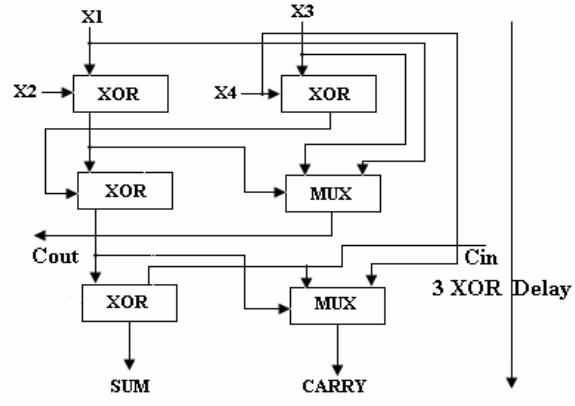

Figure 3. Alternative Implementation of 4:2 Compressor with 3 XOR Delay

3. 5-2 COMPRESSOR

The block diagram of a (5:2) compressor shown in Figure 4 has seven inputs and four outputs. Five of the inputs are the primary inputs I1, I2, I3,I4 and I5 and two other inputs, C_{inl} and C_{in2} . The architecture is connected in such a way that five of the inputs come from the same bit position of the weight j while other two inputs (C_{inl} and C_{in2}) are fed from the neighboring position j-1(known as carry-in). The outputs of 5:2 compressor consists of one bit in the position j (sum) and two bits in the position j+1 (cout1, cout2, carry). A simple implementation of the (5,2) compressor is to cascade three (3,2) full adders in a hierarchical structure, as shown in Figure 4. This architecture has a critical path delay of 6 XOR gates. Figure 5 shows another architecture of a (5:2) compressor [4]. The implementation shows that this design has a critical path delay of 4XOR + 1MUX unlike the conventional implementation with a delay of 5XOR.

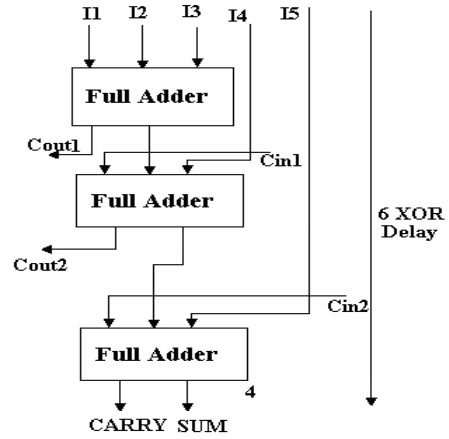

Figure 4. 5:2 Compressor using Full Adders

4. PROPOSED 4:2 AND 5-2 COMPRESSOR DESIGNS

In order to further optimize the design of the existing 4-2 and 5-2 compressor shown in Figure 3 and Figure 5, the authors propose the optimized transistor implementation of the above mentioned compressors. In the proposed compressor design, the XOR gate and MUX designs are appropriately replaced with minimum transistor implementation to design the circuit such that it has no direct supply from VDD. The optimal small area, low power, high throughput XOR design was proposed in [5] . The XOR design proposed in [5] has no power supply and is referred as Powerless XOR. Moreover , the MUX employed in the design can be implemented with 2 transistors as mentioned in [6] .Thus, it can be inferred that the proposed 4:2 compressor design is an optimized version as the authors have optimesed the entire design starting from the basic cell level. Thus, the 4-2 and 5-2 compressors are implemented with bare minimum of 20 and 30 transistors respectively.

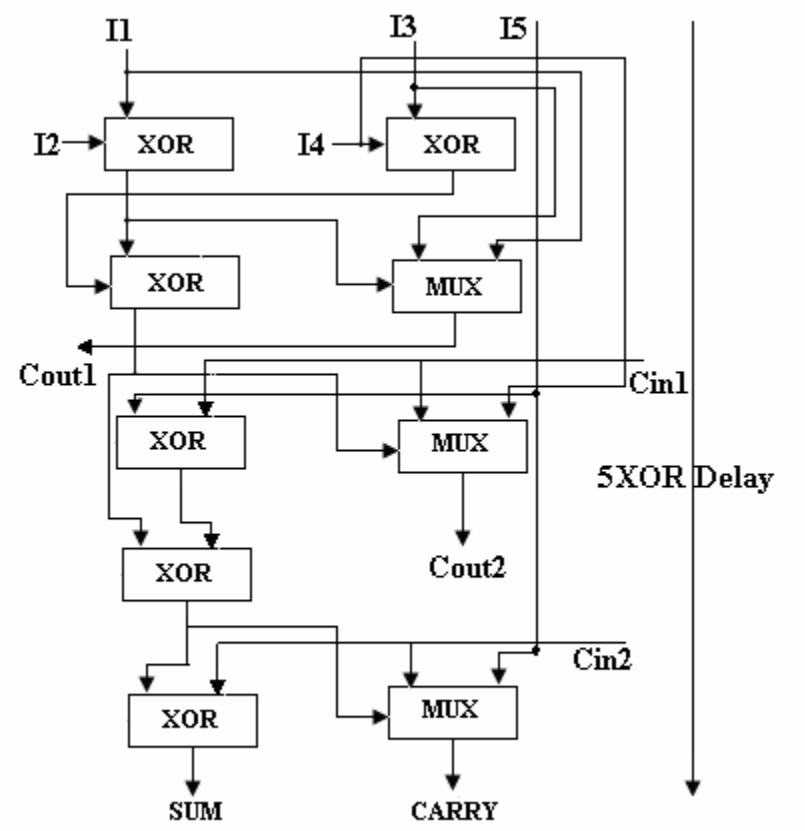

Figure 5. Alternative Implementation of 5:2 Compressor

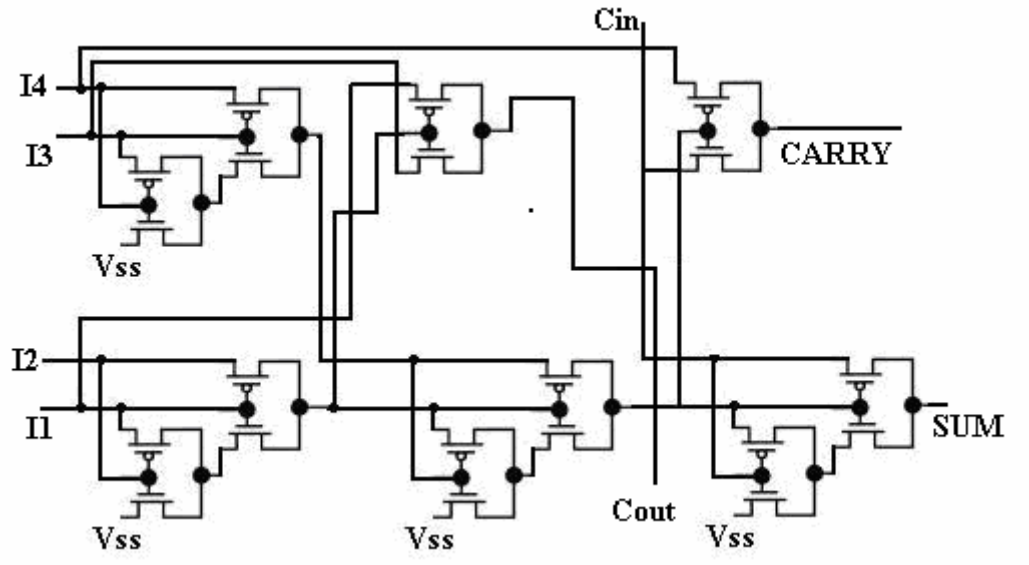

Figure 6. Transisitor level implementation of 4-2 Compressor

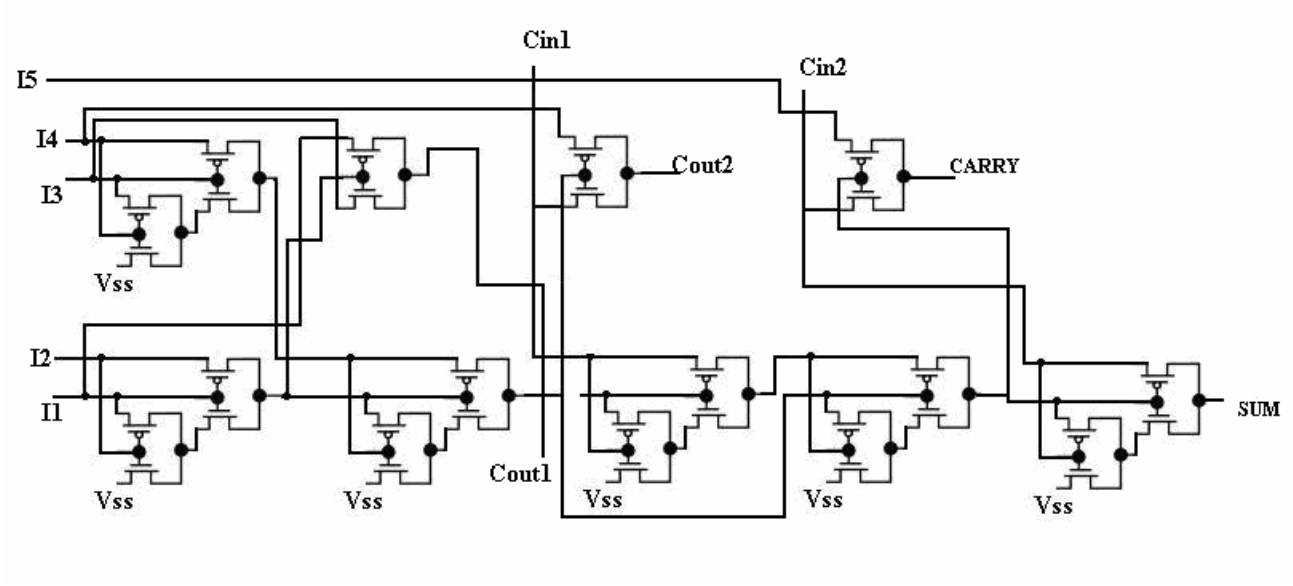

Figure 7. Transistor level implementation of 5-2 Compressor

5. THEORITICAL AND EXPERIMENTAL ANALYSIS OF THE PROPOSED DESIGNS

The evaluation of the proposed architectures is done both theoretically as well as experimentally through SPICE simulations. Since ,the proposed gates have only either VDD or GND, neither both in the same circuit, there is no short-circuit current established by a direct path between VDD and VSS. Thus, the proposed gates are highly optimized in terms of power consumption. All of its internal gate nodes are directly excited by the fresh input signals, leading to a much faster transition (low rise and fall times) in its output signals(logic transitions). Its driving capability will also be low .This along with the above advantages, makes it an ideal low power high throughput circuitry. The simulation environment is setup to measure the performance of the proposed circuits in terms of propagation delay and power dissipation. The simulations are performed by varying the frequencies of operation at various capacitive loads to ensure that the proposed circuits work at different frequencies and different capacitive loads. The Simulation conditions are shown in Figure 8.

Load	0.01 pf	0.02pf	0.05pf	0.1pf	0.3pf	0.5pf

Frequencies	10Mhz	50 Mhz	100 Mhz	200Mhz

Figure 8. Simulation Conditions

The simulation is done in Tanner spice and the technology being used is 0.35-um CMOS digital technology (TSMC 35, Canadian Microelectronic Corporation) with a 3.3-V supply voltage. The propagation delay is measured when the changing input reaches 50% of the transition to the time when the output reaches its 50%. Figures 9, 10, 11, 12 shows the power consumption and the propagation delay for a load of 0.01pf at different frequencies for the proposed 4-2 and 5-2 compressor respectively. Similarly results have been obtained for the other loading conditions.

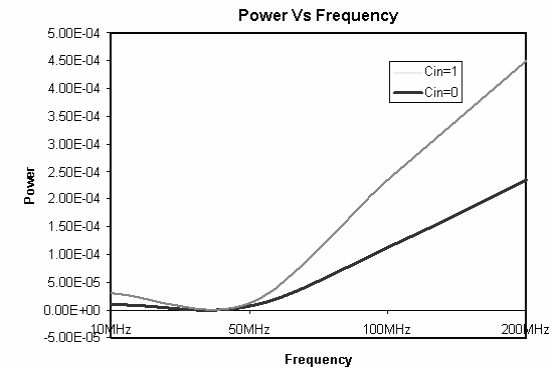

Figure 9. Power Vs Frequency for the propsed 4-2 compressor

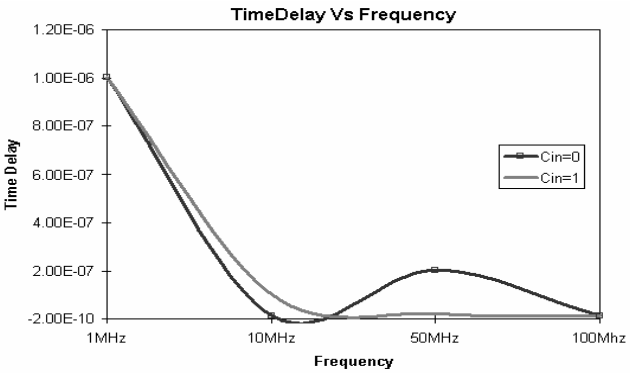

Figure 10. Time Delay Vs Freqency for the propsed 4-2 compressor

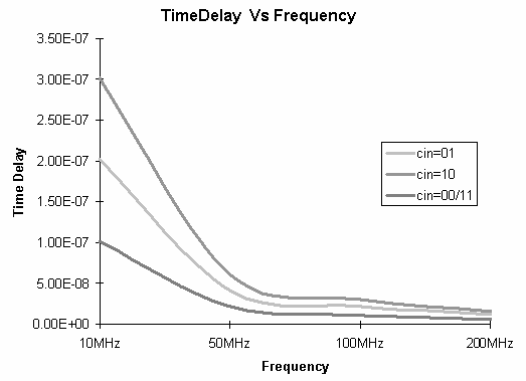

Figure 11. Time Delay Vs Frequency plot for the proposed 5-2 Compressor

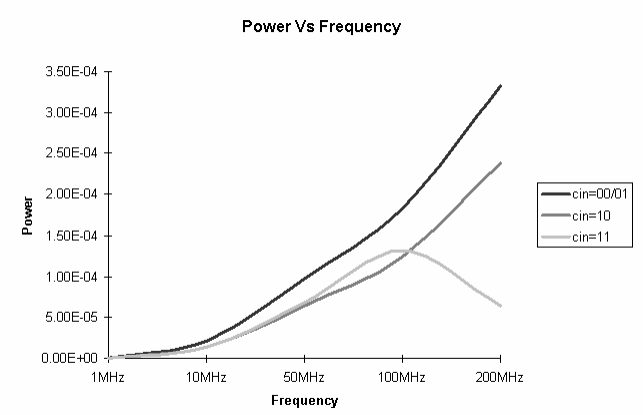

Figure 12. Power Consumption Vs Frquency plot for the proposed 5-2 Compressor

6. CONCLUSIONS

The authors have proposed two novel designs of 4-2 and 5-2 compressors .These designs were implemented with a bare minimum of 20 and 30 transistors respectively. The proposed designs have the advantage that in addition to reduced transition activity, they have no direct connections to the power-supply and are totally driven by the input signals, leading to a noticeable reduction in short-circuit power consumption. It is demonstrated that the proposed compressors designs will be highly beneficial for satisfying the need of small area low power high throughput multipliers.

REFERENCES

1. V.G. Oklobdzija, D. Villeger, S. S. Liu, “A Method for Speed Optimized Partial ProductReduction and Generation of Fast Parallel Multipliers Using and Alghoritmic Approach”, IEEE Transaction on Computers, Vol. 45, No 3, March 1996.
2. P. Stelling, C. Martel, V. G. Oklobdzija, R. Ravi, “Optimal Circuits for Parallel Multipliers”, IEEE Transaction on Computers, Vol. 47, No.3, pp. 273-285, March, 1998.
3. V. Oklobdzija, "High-Speed VLSI Arithmetic Units: Adders and Multipliers", in "Design of High-Performance Microprocessor Circuits", Book Chapter, Book edited by A. Chandrakasan, IEEE Press, 2000.
4. K. Prasad, and K.K. Parhi, “Low-power 4-2 and 5-2 compressors,” in Proc. of the 35th Asilomar Conference on Signals, Systems and Computers, vol.I, pp. 129-133,2001.
5. H. T. Bui, A. K. Al-Sheraidah, and Y. Wang, “Design and analysis of 10-transistor full adders using novel XOR-XNOR gates,” in Proc. Int. Conf. Signal Processing 2000 (World Computer Congress), Beijing, China, Aug. 2000.
6. Yingtao Jiang et.al,"A Novel Multiplexer-Based Low-Power Full Adder", IEEE Transactions on Circuits and Systems—II: Express Briefs, vol. 51, no. 7, July 2004 .